MULTIPLE TRANSMIT DATA RATES IN
PROGRAMMABLE LOGIC DEVICE SERIAL INTERFACE

Abstract of the Disclosure

[0036] A serial interface for a programmable logic device provides multiple data rates in different channels by generating a central serial clock and providing at least one divider in each channel that can divide the central clock by different integer values. For additional variation in clock rate, two or more different central clocks can be provided, with each channel then being able to divide any of the central clocks to provide the desired local clock. Lower speed parallel clocks can be generated locally by further dividing the divided serial clock. Alternatively, the central serial clock or clocks may be divided centrally to provide a central parallel clock or clocks which can then be used locally as a local parallel clock.